A11 amd

33. (Amended) The method of Claim 29, wherein the hardmask layer comprises a material comprising silicon oxynitride and silicon oxide.

A12

35. (Amended) The method of Claim 22 wherein said conducting material comprises aluminum, copper, tungsten, and mixtures thereof.

A13

37. (Amended) The method of Claim 22 wherein said substrate comprises semiconductor wafers, dielectric layers, or metal interconnect layers in integrated circuits.

IN THE SPECIFICATION

Please amend the original specification on page 5, line 20 to replace the text --Figures 2a-2g-- with the text --Figures 2a-2h--.

A14

REMARKS

35 USC § 112

Claims 4-7, 10-12, 16, 28 and 31-33 were rejected under 35 USC §112 as being indefinite. The Applicant disagrees, especially in view of the amendments made herein.

Claim 4 is amended herein to remove the phrase "and oligomers". Therefore, claim 4 is allowable as being supported by the original specification. Claims 5-7 are also therefore allowable as being based on definite claim 4.

Claims 10 and 31 are amended herein to remove the reference to silicon nitride and mixtures of silicon nitride. Therefore, claims 10 and 31 are herein allowable as being definite.

Claims 11 and 32 are specifically supported by the original specification. The "second organic intermetal dielectric layer" is defined on original specification page 7, lines 1-10 where it recites that "Organic intermetal dielectric **layers** used in the methods of the present invention..." (emphasis added). Clearly, each organic intermetal dielectric layer contemplated in the specification is defined by the text on page 7, lines 1-10 of the original specification. This part

of the specification does not specifically refer to either the first or second organic intermetal dielectric layer, **but instead refers to both layers in a generic sense**. Therefore, claims 11 and 32 are allowable as being definite.

Claims 7, 12, 16, 28 and 33 are herein amended to remove the term "mixtures". Therefore, these claims are herein allowable as being definite.

Therefore, based on the arguments and amendments presented herein, claims 2, 4-8, 19 and 20 are allowable as being definite and for particularly pointing out and distinctly claiming the subject matter which applicant regards as the invention.

35 USC § 102

Claims 22, 25, 35 and 37 were rejected under 35 USC § 102(b) as being anticipated by Avanzino et al. (US 5,795,823). The applicant disagrees.

Claim 22 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer; b) forming a line opening in said stack; c) depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and **covering the top surface of the stack**; d) **depositing a photoresist material on the sacrificial inorganic dielectric**; e) **developing the photoresist material**; f) forming a via opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material. In other words, after the sacrificial inorganic dielectric is deposited in the line opening and on top of the stack, a photoresist material is deposited on the dielectric and developed.

The methods taught in Avanzino do not teach or suggest that the conformal material is applied in the line opening **and** on top of the layered stack. There is also nothing in the description of Avanzino that would teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack.

The methods taught in Avanzino also specifically teach against an additional photoresist application step after the conformal material is deposited in the line opening. The sidewalls created by an etch step actually serve as a self-aligning mask – and thus, there is no need for another photoresist application step. (See Abstract). The rule regarding "teaching against" is that a reference that teaches against the claimed subject matter can only be used to establish obviousness if there is something in the prior art that would have caused those skilled in the art to disregard the teachings of the reference in order to produce the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.,* 721 F.2d 1540, 1552, 220 U.S.P.Q. 303, 314 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851, 83 L. Ed. 2d 107, 105 S. Ct. 172 (1984).

> "The result is that the claims were used as a frame, and individual, naked parts of separate prior art references were employed as a mosaic to recreate a facsimile of the claimed invention. At no point did the district court, nor does Garlock, explain why that mosaic would have been obvious to one skilled in the art in 1969, or what there was in the prior art that would have caused those skilled in the art to disregard the teachings there found against making just such a mosaic."

In this instance, Avanzino teaches against the presently claimed subject matter, and there is nothing in the prior art that would lead one of ordinary skill to disregard such teachings.

Therefore, the methods taught in the specification and claims of Avanzino could not anticipate the methods of the present application, since Avanzino does not teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack and also since Avanzino does not teach or suggest that an additional photoresist material is applied and developed on the layered stack **after the application** of the conformal fill material.

Based on these arguments, among others, claim 22 is allowable as not being anticipated by Avanzino. Further, claims 25, 35 and 37 are also allowable as being dependent on independent claim 22.

35 USC § 103

Claims 1-6, 8-11, 13-15 and 17-21 were rejected under 35 USC § 103(a) as being unpatentable over the admitted prior art in view of Avanzino et al. (US 5,795,823) and Pellerin et al. The applicant disagrees.

Claim 1 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer; b) forming a via opening in said stack; c) depositing a sacrificial inorganic dielectric in the via opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and **covering the top surface of the stack**; d) **depositing a photoresist material on the sacrificial inorganic dielectric**; e) **developing the photoresist material**; f) forming a line opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material. In other words, after the sacrificial inorganic dielectric is deposited in the via opening and on top of the stack, a photoresist material is deposited on the dielectric and developed.

The methods taught in Avanzino do not teach or suggest that the conformal material is applied in the via opening **and** on top of the layered stack. There is also nothing in the description of Avanzino that would teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack. The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply the conformal material to the via opening and to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that the conformal material can or should be applied simultaneously to the via opening and the top of the stack.

Further, the methods taught in Avanzino also specifically teach against an additional photoresist application step after the conformal material is deposited in the line opening. The rule regarding "teaching against" is that a reference that teaches against the claimed subject matter can only be used to establish obviousness if there is something in the prior art that would

have caused those skilled in the art to disregard the teachings of the reference in order to produce the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1552, 220 U.S.P.Q. 303, 314 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851, 83 L. Ed. 2d 107, 105 S. Ct. 172 (1984).

> "The result is that the claims were used as a frame, and individual, naked parts of separate prior art references were employed as a mosaic to recreate a facsimile of the claimed invention. At no point did the district court, nor does Garlock, explain why that mosaic would have been obvious to one skilled in the art in 1969, or what there was in the prior art that would have caused those skilled in the art to disregard the teachings there found against making just such a mosaic."

In this instance, Avanzino teaches against the presently claimed subject matter, and there is nothing in the prior art that would lead one of ordinary skill to disregard such teachings. The sidewalls created by an etch step actually serve as a self-aligning mask – and thus, there is no need for another photoresist application step. (See Abstract). The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply an additional photoresist material to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that an extra photoresist material or step should be applied to the top of the stack.

Therefore, the methods taught in the specification and claims of Avanzino do not teach, suggest or motivate one of ordinary skill in the art of interconnect assembly to contemplate the methods of the present application, since Avanzino does not teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack and also since Avanzino does not teach or suggest that an additional photoresist material is applied and developed on the layered stack **after the application** of the conformal fill material.

The methods taught in Pellerin also do not teach or suggest that a hardmask layer or etch stop layer is present in the stack on the substrate. As a matter of fact, Pellerin teaches against an etch stop or hardmask layer in his layered stack in the background as support for the novelty of his method – which specifically does not incorporate a hardmask or etch stop layer. Therefore, it

would not be obvious to one of ordinary skill in the art of interconnect assembly to use Pellerin as a guide for producing the methods contemplated by the present application.

Based on these arguments, among others, claim 1 is allowable as being patentable over Avanzino in view of Pellerin. Further, claims 2-6, 8-11, 13-15 and 17-21 are also allowable as being dependent on independent claim 1.

Claims 23-24, 34 and 36 were rejected under 35 USC § 103(a) as being unpatentable over the admitted prior art in view of Avanzino et al. (US 5,795,823) as applied to claim 22, and further in view of Pellerin et al. The applicant disagrees.

Claim 22 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer; b) forming a line opening in said stack; c) depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and **covering the top surface of the stack**; d) **depositing a photoresist material on the sacrificial inorganic dielectric**; e) **developing the photoresist material**; f) forming a via opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material. In other words, after the sacrificial inorganic dielectric is deposited in the line opening and on top of the stack, a photoresist material is deposited on the dielectric and developed.

The methods taught in Avanzino do not teach or suggest that the conformal material is applied in the line opening **and** on top of the layered stack. There is also nothing in the description of Avanzino that would teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack. The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply the conformal material to the line opening and to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that the conformal material can or should be applied simultaneously to the line opening and the top of

the stack.

Further, the methods taught in Avanzino also specifically teach against an additional photoresist application step after the conformal material is deposited in the line opening. The rule regarding "teaching against" is that a reference that teaches against the claimed subject matter can only be used to establish obviousness if there is something in the prior art that would have caused those skilled in the art to disregard the teachings of the reference in order to produce the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1552, 220 U.S.P.Q. 303, 314 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851, 83 L. Ed. 2d 107, 105 S. Ct. 172 (1984).

> "The result is that the claims were used as a frame, and individual, naked parts of separate prior art references were employed as a mosaic to recreate a facsimile of the claimed invention. At no point did the district court, nor does Garlock, explain why that mosaic would have been obvious to one skilled in the art in 1969, or what there was in the prior art that would have caused those skilled in the art to disregard the teachings there found against making just such a mosaic."

In this instance, Avanzino teaches against the presently claimed subject matter, and there is nothing in the prior art that would lead one of ordinary skill to disregard such teachings. The sidewalls created by an etch step actually serve as a self-aligning mask – and thus, there is no need for another photoresist application step. (See Abstract). The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply an additional photoresist material to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that an extra photoresist material or step should be applied to the top of the stack.

Therefore, the methods taught in the specification and claims of Avanzino do not teach, suggest or motivate one of ordinary skill in the art of interconnect assembly to contemplate the methods of the present application, since Avanzino does not teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack and also since

Avanzino does not teach or suggest that an additional photoresist material is applied and developed on the layered stack **after the application** of the conformal fill material.

The methods taught in Pellerin also do not teach or suggest that a hardmask layer or etch stop layer is present in the stack on the substrate. As a matter of fact, Pellerin teaches against an etch stop or hardmask layer in his layered stack in the background as support for the novelty of his method – which specifically does not incorporate a hardmask or etch stop layer. Therefore, it would not be obvious to one of ordinary skill in the art of interconnect assembly to use Pellerin as a guide for producing the methods contemplated by the present application.

Based on these arguments, among others, claim 22 is allowable as being patentable over Avanzino in view of Pellerin. Further, claims 23-24, 34 and 36 are also allowable as being dependent on independent claim 22.

Claims 26-27, 29-32 and 38 were rejected under 35 USC § 103(a) as being unpatentable over the admitted prior art in view of Avanzino et al. (US 5,795,823) (assumed to be as applied to claim 22). The applicant disagrees.

Claim 22 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer; b) forming a line opening in said stack; c) depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and covering the top surface of the stack; d) depositing a photoresist material on the sacrificial inorganic dielectric; e) developing the photoresist material; f) forming a via opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material. In other words, after the sacrificial inorganic dielectric is deposited in the line opening and on top of the stack, a photoresist material is deposited on the dielectric and developed.

The methods taught in Avanzino do not teach or suggest that the conformal material is applied in the line opening **and** on top of the layered stack. There is also nothing in the

description of Avanzino that would teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack. The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply the conformal material to the line opening and to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that the conformal material can or should be applied simultaneously to the line opening and the top of the stack.

Further, the methods taught in Avanzino also specifically teach against an additional photoresist application step after the conformal material is deposited in the line opening. The rule regarding "teaching against" is that a reference that teaches against the claimed subject matter can only be used to establish obviousness if there is something in the prior art that would have caused those skilled in the art to disregard the teachings of the reference in order to produce the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1552, 220 U.S.P.Q. 303, 314 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851, 83 L. Ed. 2d 107, 105 S. Ct. 172 (1984).

> "The result is that the claims were used as a frame, and individual, naked parts of separate prior art references were employed as a mosaic to recreate a facsimile of the claimed invention. At no point did the district court, nor does Garlock, explain why that mosaic would have been obvious to one skilled in the art in 1969, or what there was in the prior art that would have caused those skilled in the art to disregard the teachings there found against making just such a mosaic."

In this instance, Avanzino teaches against the presently claimed subject matter, and there is nothing in the prior art that would lead one of ordinary skill to disregard such teachings. The sidewalls created by an etch step actually serve as a self-aligning mask – and thus, there is no need for another photoresist application step. (See Abstract). The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply an additional photoresist material to the top of the layered stack, given that no part of the extensive

examples, the detailed description or the claims in Avanzino disclose or teach that an extra photoresist material or step should be applied to the top of the stack.

Therefore, the methods taught in the specification and claims of Avanzino do not teach, suggest or motivate one of ordinary skill in the art of interconnect assembly to contemplate the methods of the present application, since Avanzino does not teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack and also since Avanzino does not teach or suggest that an additional photoresist material is applied and developed on the layered stack **after the application** of the conformal fill material.

Based on these arguments, among others, claim 22 is allowable as being patentable over Avanzino. Further, claims 26-27, 29-32 and 38 are also allowable as being dependent on independent claim 22.

Claims 7, 12 and 16 were rejected under 35 USC § 103(a) as being unpatentable over the admitted prior art in view of Avanzino et al. (US 5,795,823) and Pellerin et al, as applied to claim 1 above, and further in view of Huang et al. (US 5,635,423). The applicant disagrees.

Claim 1 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer; b) forming a via opening in said stack; c) depositing a sacrificial inorganic dielectric in the via opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and **covering the top surface of the stack**; d) **depositing a photoresist material on the sacrificial inorganic dielectric**; e) **developing the photoresist material**; f) forming a line opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material. In other words, after the sacrificial inorganic dielectric is deposited in the via opening and on top of the stack, a photoresist material is deposited on the dielectric and developed.

The methods taught in Avanzino do not teach or suggest that the conformal material is

applied in the via opening **and** on top of the layered stack. There is also nothing in the description of Avanzino that would teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack. The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply the conformal material to the via opening and to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that the conformal material can or should be applied simultaneously to the via opening and the top of the stack.

Further, the methods taught in Avanzino also specifically teach against an additional photoresist application step after the conformal material is deposited in the line opening. The rule regarding "teaching against" is that a reference that teaches against the claimed subject matter can only be used to establish obviousness if there is something in the prior art that would have caused those skilled in the art to disregard the teachings of the reference in order to produce the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1552, 220 U.S.P.Q. 303, 314 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851, 83 L. Ed. 2d 107, 105 S. Ct. 172 (1984).

> "The result is that the claims were used as a frame, and individual, naked parts of separate prior art references were employed as a mosaic to recreate a facsimile of the claimed invention. At no point did the district court, nor does Garlock, explain why that mosaic would have been obvious to one skilled in the art in 1969, or what there was in the prior art that would have caused those skilled in the art to disregard the teachings there found against making just such a mosaic."

In this instance, Avanzino teaches against the presently claimed subject matter, and there is nothing in the prior art that would lead one of ordinary skill to disregard such teachings. The rule regarding "teaching against" is that a reference that teaches against the claimed subject matter can only be used to establish obviousness if there is something in the prior art that would have caused those skilled in the art to disregard the teachings of the reference in order to produce

the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1552, 220 U.S.P.Q. 303, 314 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851, 83 L. Ed. 2d 107, 105 S. Ct. 172 (1984).

> "The result is that the claims were used as a frame, and individual, naked parts of separate prior art references were employed as a mosaic to recreate a facsimile of the claimed invention. At no point did the district court, nor does Garlock, explain why that mosaic would have been obvious to one skilled in the art in 1969, or what there was in the prior art that would have caused those skilled in the art to disregard the teachings there found against making just such a mosaic."

In this instance, Avanzino teaches against the presently claimed subject matter, and there is nothing in the prior art that would lead one of ordinary skill to disregard such teachings. The sidewalls created by an etch step actually serve as a self-aligning mask – and thus, there is no need for another photoresist application step. (See Abstract). The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply an additional photoresist material to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that an extra photoresist material or step should be applied to the top of the stack.

Therefore, the methods taught in the specification and claims of Avanzino do not teach, suggest or motivate one of ordinary skill in the art of interconnect assembly to contemplate the methods of the present application, since Avanzino does not teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack and also since Avanzino does not teach or suggest that an additional photoresist material is applied and developed on the layered stack **after the application** of the conformal fill material.

The methods taught in Pellerin also do not teach or suggest that a hardmask layer or etch stop layer is present in the stack on the substrate. As a matter of fact, Pellerin teaches against an etch stop or hardmask layer in his layered stack in the background as support for the novelty of his method – which specifically does not incorporate a hardmask or etch stop layer. Therefore, it

would not be obvious to one of ordinary skill in the art of interconnect assembly to use Pellerin as a guide for producing the methods contemplated by the present application.

The methods taught in Huang do not teach or suggest using a sacrificial inorganic dielectric material to fill the line or via opening and cover the top of the stack. Huang uses a method to simultaneously form a trench and fill the trench with conductive material – thereby bypassing the step of using an inorganic dielectric material. Based on the disclosure in Huang, it is not clear to the Applicant why this reference should even be used in combination with Avanzino and/or Pellerin. Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. See, e.g., *C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1352, 48 U.S.P.Q.2D (BNA) 1225, 1232 (Fed. Cir. 1998)* (describing "teaching or suggestion or motivation [to combine]" as an "essential evidentiary component of an obviousness holding"); *In re Rouffet, 149 F.3d 1350, 1359, 47 U.S.P.Q.2D (BNA) 1453, 1459 (Fed. Cir. 1998)* ("the Board must identify specifically . . . the reasons one of ordinary skill in the art would have been motivated to select [**11] the references and combine them"); *In re Fritch, 972 F.2d 1260, 1265, 23 U.S.P.Q.2D (BNA) 1780, 1783 (Fed. Cir. 1992)* (**examiner can satisfy burden of obviousness in light of combination "only by showing some objective teaching [leading to the combination]**"); *In re Fine, 837 F.2d 1071, 1075, 5 U.S.P.Q.2D (BNA) 1596, 1600 (Fed. Cir. 1988)* (evidence of teaching or suggestion "essential" to avoid hindsight); *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 297, 227 U.S.P.Q. (BNA) 657, 667 (Fed. Cir. 1985)* (district court's conclusion of obviousness was error when it "did not elucidate any factual teachings, suggestions or incentives from this prior art that showed the propriety of combination"). See also *Graham, 383 U.S. at 18, 148 U.S.P.Q. (BNA) at 467* ("strict observance" of factual predicates to obviousness conclusion required). Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight. See, e.g., *Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 U.S.P.Q. (BNA) 543, 547 (Fed. Cir. 1985)* ("The invention [**12] must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."). In this case, the Board fell into the hindsight trap. In re Anita Dembriczak

et al., 175 F.3d 994; 50 U.S.P.Q.2D 1614, (Fed. Cir. 1999).

Therefore, it would not be obvious to one of ordinary skill in the art to consider Huang as a relevant reference when considering a process of using a sacrificial inorganic dielectric material to help form a line opening and via opening, since one of ordinary skill in the art would not have found it obvious to include Huang as a reference in those that might be related to the use of sacrificial inorganic dielectric materials or the present invention.

Based on these arguments, among others, claim 1 is allowable as being patentable over Avanzino in view of Pellerin and Huang. Further, claims 7, 12 and 16 are also allowable as being dependent on independent claim 1.

Claims 28 and 33 were rejected under 35 USC § 103(a) as being unpatentable over the admitted prior art in view of Avanzino et al. (US 5,795,823) and further in view of Huang et al. (US 5,635,423). The applicant disagrees.

Claim 22 recites a method of making conducting vias and conducting lines on a substrate that comprises: a) depositing a stack having a top surface on a substrate, wherein the stack comprises a first organic intermetal dielectric layer; b) forming a line opening in said stack; c) depositing a sacrificial inorganic dielectric in the line opening, wherein the sacrificial inorganic dielectric substantially filling the line opening and covering the top surface of the stack; d) depositing a photoresist material on the sacrificial inorganic dielectric; e) developing the photoresist material; f) forming a via opening in the stack and the sacrificial inorganic dielectric; g) selectively removing the sacrificial inorganic dielectric; and h) filling the via opening and the line opening with conducting material. In other words, after the sacrificial inorganic dielectric is deposited in the line opening and on top of the stack, a photoresist material is deposited on the dielectric and developed.

The methods taught in Avanzino do not teach or suggest that the conformal material is applied in the line opening **and** on top of the layered stack. There is also nothing in the description of Avanzino that would teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack. The methods taught in Avanzino would

also not motivate one ordinarily skilled in the art of interconnect assembly to apply the conformal material to the line opening and to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that the conformal material can or should be applied simultaneously to the line opening and the top of the stack.

Further, the methods taught in Avanzino also specifically teach against an additional photoresist application step after the conformal material is deposited in the line opening. The sidewalls created by an etch step actually serve as a self-aligning mask – and thus, there is no need for another photoresist application step. (See Abstract). The methods taught in Avanzino would also not motivate one ordinarily skilled in the art of interconnect assembly to apply an additional photoresist material to the top of the layered stack, given that no part of the extensive examples, the detailed description or the claims in Avanzino disclose or teach that an extra photoresist material or step should be applied to the top of the stack.

Therefore, the methods taught in the specification and claims of Avanzino do not teach, suggest or motivate one of ordinary skill in the art of interconnect assembly to contemplate the methods of the present application, since Avanzino does not teach or suggest that the conformal material can be or is intended to be applied to the top of the layered stack and also since Avanzino does not teach or suggest that an additional photoresist material is applied and developed on the layered stack **after the application** of the conformal fill material.

The methods taught in Huang do not teach or suggest using a sacrificial inorganic dielectric material to fill the line or via opening and cover the top of the stack. Huang uses a method to simultaneously form a trench and fill the trench with conductive material – thereby bypassing the step of using an inorganic dielectric material. Based on the disclosure in Huang, it is not clear to the Applicant why this reference should even be used in combination with Avanzino and/or Pellerin. Our case law makes clear that the best defense against the subtle but powerful attraction of a hindsight-based obviousness analysis is rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references. See, e.g., *C.R. Bard, Inc. v. M3 Sys., Inc., 157 F.3d 1340, 1352, 48 U.S.P.Q.2D (BNA) 1225, 1232 (Fed. Cir. 1998)* (describing "teaching or suggestion or motivation [to combine]" as an "essential

evidentiary component of an obviousness holding"); *In re Rouffet, 149 F.3d 1350, 1359, 47 U.S.P.Q.2D (BNA) 1453, 1459 (Fed. Cir. 1998)* ("the Board must identify specifically . . . the reasons one of ordinary skill in the art would have been motivated to select [**11] the references and combine them"); *In re Fritch, 972 F.2d 1260, 1265, 23 U.S.P.Q.2D (BNA) 1780, 1783 (Fed. Cir. 1992)* (**examiner can satisfy burden of obviousness in light of combination "only by showing some objective teaching [leading to the combination]**"); *In re Fine, 837 F.2d 1071, 1075, 5 U.S.P.Q.2D (BNA) 1596, 1600 (Fed. Cir. 1988)* (evidence of teaching or suggestion "essential" to avoid hindsight); *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 297, 227 U.S.P.Q. (BNA) 657, 667 (Fed. Cir. 1985)* (district court's conclusion of obviousness was error when it "did not elucidate any factual teachings, suggestions or incentives from this prior art that showed the propriety of combination"). See also *Graham, 383 U.S. at 18, 148 U.S.P.Q. (BNA) at 467* ("strict observance" of factual predicates to obviousness conclusion required). Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability--the essence of hindsight. See, e.g., *Interconnect Planning Corp. v. Feil, 774 F.2d 1132, 1138, 227 U.S.P.Q. (BNA) 543, 547 (Fed. Cir. 1985)* ("The invention [**12] must be viewed not with the blueprint drawn by the inventor, but in the state of the art that existed at the time."). In this case, the Board fell into the hindsight trap. In re Anita Dembriczak et al., 175 F.3d 994; 50 U.S.P.Q.2D 1614, (Fed. Cir. 1999).

Therefore, it would not be obvious to one of ordinary skill in the art to consider Huang as a relevant reference when considering a process of using a sacrificial inorganic dielectric material to help form a line opening and via opening, since one of ordinary skill in the art would not have found it obvious to include Huang as a reference in those that might be related to the use of sacrificial inorganic dielectric materials or the present invention.

Based on these arguments, among others, claim 22 is allowable as being patentable over Avanzino. Further, claims 28 and 33 are also allowable as being dependent on independent claim 22.

REQUEST FOR ALLOWANCE

Claims 1-38 are pending in this application. The applicant requests allowance of all pending claims.

Respectfully submitted,

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1. (Amended) A method of making conducting vias and conducting lines on a substrate comprising:

depositing a stack having a top surface on a substrate, wherein the [said] stack comprises a first organic intermetal dielectric layer and a hardmask layer;

forming a via opening in said stack;

depositing a sacrificial inorganic dielectric in the [said] via opening, wherein the [said] sacrificial inorganic dielectric substantially filling the [said] via opening and substantially covering the top surface of the stack;

depositing a photoresist material on the sacrificial inorganic dielectric;

developing the photoresist material;

forming a line opening in the [said]stack and the [said] sacrificial inorganic dielectric, said line opening substantially aligned with said via opening;

selectively removing the [said] sacrificial inorganic dielectric; and

filling the [said] via opening and the [said] line opening with conducting material.

2. (Amended) The method of Claim 1 wherein said sacrificial inorganic dielectric [is selected from the group consisting of] comprises methylsiloxanes, phenylsiloxanes, methylphenylsiloxanes, methylsilsesquioxanes, methylphenylsilsesquioxanes, silicates, perhydrosilazanes, hydridosiloxanes [and] or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, and mixtures thereof.

3. The method of Claim 1 wherein said sacrificial inorganic dielectric is a methylsiloxane.

4. (Amended) The method of Claim 1, wherein the [said] organic intermetal dielectric layer

comprises an organic dielectric [selected from the group comprising] that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers [and oligomers], fluorinated amorphous carbon, and mixtures thereof.

5. The method of Claim 1 wherein said stack further comprises a diffusion barrier layer between said substrate and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

6. The method of Claim 5 wherein said diffusion barrier layer comprises silicon nitride.

7. (Amended) The method of claim 5, wherein the [said] hardmask layer comprises a material comprising silicon oxynitride[,] and silicon oxide [,and mixtures thereof].

8. The method of Claim 1 wherein said stack further comprises:

a diffusion barrier layer between said substrate and said organic intermetal dielectric layer;

an etchstop layer on said intermetal organic dielectric layer;

a second organic intermetal dielectric layer on said etchstop layer; and

a hardmask layer on said second intermetal dielectric layer.

9. The method of Claim 8 wherein said diffusion barrier layer comprises silicon nitride.

10. (Amended) The method of claim 8, wherein the [said] etchstop layer comprises a material comprising silicon oxide [,silicon nitride, and mixtures thereof].

11. (Amended) The method of Claim 8, wherein the [said] second organic intermetal dielectric layer comprises an organic dielectric [selected from the group comprising] that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers [and oligomers], fluorinated amorphous carbon, and mixtures thereof.

12. (Amended) The method of claim 8, wherein the [said] hardmask layer comprises a material comprising silicon oxynitride[,] and silicon oxide [,and mixtures thereof].

13. The method of Claim 1 wherein said stack further comprises a diffusion barrier layer on said substrate, and inorganic intermetal dielectric layer between said diffusion barrier and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

14. The method of Claim 13 wherein said diffusion barrier layer comprises silicon nitride.

15. (Amended) The method of clam 13 wherein said inorganic intermetal dielectric layer comprises a material [selected from the group consisting of] that comprises silicon oxide, fluorinated silicate glass, or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, and mixtures thereof.

16. (Amended) The method of claim 13, wherein the [said] hardmask layer comprises a material comprising silicon oxynitride[,] and silicon oxide [,and mixtures thereof].

17. The method of Claim 1 wherein said sacrificial inorganic dielectric is selectively removed with a buffered oxide etch.

18. (Amended) The method of Claim 1 wherein said conducting material comprises [a metal selected from the group consisting of] aluminum, copper, tungsten, and mixtures thereof.

19. The method of Claim 18 wherein said conducting material further comprises a conducting diffusion barrier material.

20. (Amended) The method of Claim 1 wherein said substrate [is selected from the group consisting of] comprises semiconductor wafers, dielectric layers, [and] or metal interconnect layers in integrated circuits.

21. The method of Claim 1 wherein said via openings and said line openings are formed by etching with an oxygen based plasma and with a fluorocarbon based plasma.

22. (Amended) A method of making conducting vias and conducting lines on a substrate comprising:

depositing a stack having a top surface on a substrate, wherein the [said] stack comprises a first organic intermetal dielectric layer and a hardmask layer;

forming a line opening in said stack;

depositing a sacrificial inorganic dielectric in the [said] line opening, wherein the [said] sacrificial inorganic dielectric substantially filling the [said] line opening and substantially covering the top surface of the stack;

depositing a photoresist material on the sacrificial inorganic dielectric;

developing the photoresist material;

forming a via opening in the [said] stack and the [said] sacrificial inorganic dielectric;

selectively removing the [said] sacrificial inorganic dielectric; and

filling the [said] via opening and the [said] line opening with conducting material.

23. (Amended) The method of Claim 22 wherein said sacrificial inorganic dielectric [is selected from the group consisting of] comprises methylsiloxanes, phenylsiloxanes, methylphenylsiloxanes, methylsilsesquioxanes, methylphenylsilsesquioxanes, silicates, perhydrosilazanes, hydridosiloxanes [and] or organohydridosiloxanes described by the general formula $(H_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_n(R_{0.4\text{-}1.0}SiO_{1.5\text{-}1.8})_m$ wherein the sum of n and m is from about 8 to about 5000, and mixtures thereof.

24. The method of Claim 22 wherein said sacrificial inorganic dielectric is a methylsiloxane.

25. (Amended) The method of Claim 22, wherein the [said] organic intermetal dielectric layer comprises an organic dielectric [selected from the group comprising] that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic

monomers [and oligomers], fluorinated amorphous carbon, and mixtures thereof.

26. The method of Claim 22 wherein said stack further comprises a diffusion barrier layer between said substrate and said organic intermetal dielectric layer, and a hardmask layer on said organic intermetal dielectric layer.

27. The method of Claim 26 wherein said diffusion barrier layer comprises silicon nitride.

28. (Amended) The method of claim 26, wherein the [said] hardmask layer comprises a material comprising silicon oxynitride[,] and silicon oxide [,and mixtures thereof].

29. The method of Claim 22 wherein said stack further comprises:

a diffusion barrier layer between said substrate and said organic intermetal dielectric layer;

an etchstop layer on said intermetal organic dielectric layer;

a second organic intermetal dielectric layer on said etchstop layer; and

a hardmask layer on said second intermetal dielectric layer.

30. The method of Claim 29 wherein said diffusion barrier layer comprises silicon nitride.

31. (Amended) The method of claim 29, wherein the [said] etchstop layer comprises a material comprising silicon oxide [,silicon nitride, and mixtures thereof].

32. (Amended) The method of Claim 29, wherein the [said] second organic intermetal dielectric layer comprises an organic dielectric [selected from the group consisting of] that comprises polyimides, polytetrafluoroethylene, parylenes, fluorinated and non fluorinated poly(arylene ethers), polymeric material obtained from phenyl-ethynylated aromatic monomers [and oligomers], fluorinated amorphous carbon, and mixtures thereof.

33. (Amended) The method of claim 29, wherein the [said] hardmask layer comprises a material comprising silicon oxynitride[,] and silicon oxide [,and mixtures thereof].

34. The method of Claim 22 wherein said sacrificial inorganic dielectric is selectively removed with a buffered oxide etch.

35. (Amended) The method of Claim 22 wherein said conducting material comprises [a metal selected from the group consisting of] aluminum, copper, tungsten, and mixtures thereof.

36. The method of Claim 35 wherein said conducting material further comprises a conducting diffusion barrier material.

37. (Amended) The method of Claim 22 wherein said substrate [is selected from the group consisting of] comprises semiconductor wafers, dielectric layers, [and] or metal interconnect layers in integrated circuits.

38. The method of Claim 22 wherein said via openings and said line openings are formed by etching with an oxygen based plasma and with a fluorocarbon based plasma.